

How Non-Volatile Memory Became the World's Most Valuable Semiconductor Storage **A Conversation with Eli Harari, Stefan Lai and Jeff Katz**

Led by Brian Berg
**Chair, IEEE SCV Technology History
Committee; R6 Milestone Coordinator**
30 September 2015



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Doron Noyman will say a few words



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Our Panel of Speakers: Dr. Eli Harari

- Worked at Intel ('79-'81); 1988: founded SunDisk (renamed SanDisk) - was CEO and Chairman
- 150 issued patents; many technical papers
- 2004 Ernst & Young Entrepreneur of the Year Lifetime Award
- 2006 IEEE Reynold B. Johnson Data Storage Device Tech. Award
- 2008 GSA (Global Semiconductor Alliance) Dr. Morris Chang Exemplary Leadership Award
- 2009 IEEE Robert N. Noyce Medal for Exceptional Contributions to the Microelectronics Industry
- 2011: Consumer Electronics Hall of Fame
- Member: National Academy of Engineering
- 2014: National Medal of Technology and Innovation (from President Obama)



Our Panel of Speakers: Dr. Stefan Lai

- IBM (1979-1982): researched silicon-silicon dioxide interface properties at IBM Yorktown TJ Watson Research Center
- Intel (1982-2006): developed scalable EEPROM; co-invented the hugely successful EPROM tunnel oxide (ETOX) flash memory cell
- Through 10 generations of ETOX technologies (1983-2006), achieved 1000X cell size reduction
- 1998: IEEE Fellow for “distinguished research on the properties of silicon MOS interfaces and development of Flash EPROM Memory”
- 2008: IEEE Andrew S. Grove Award for “contributions to the development and advancement of flash memory technology that has spurred the success and popularity of several consumer electronics devices including the USB flash drive”



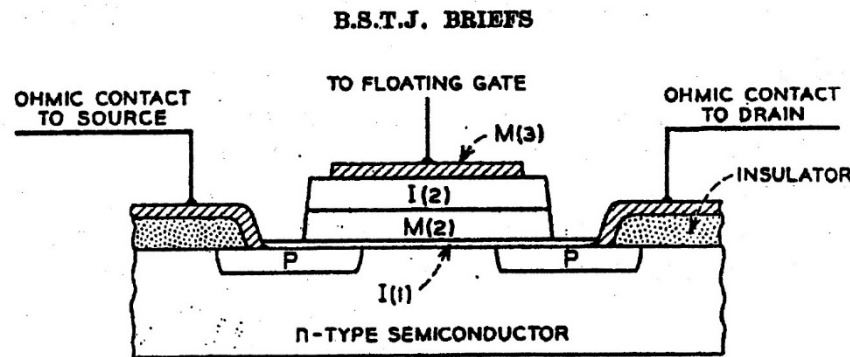
Our Panel of Speakers: Jeff Katz

- At Intel (1977-1987) and Atmel (1988-2005):
 - At Intel, served in various microprocessor, microcontroller, ASIC and memory Marketing and Operational roles
 - At Atmel, served as Chief Marketing Officer and did product definition and market development for a broad range of non-volatile memories (including EPROM, EEPROM and Flash) as well as several families of Flash-based microcontrollers
- Computer History Museum (CHM) (2004-present):
 - Instrumental in CHM's Semiconductor Special Interest Group, which collects artifacts and Oral Histories of seminal chip products
 - Has captured the human and technical stories of virtually every key NVM technology innovator
 - Has led Oral Histories of Charles Sie, Simon Sze, Dov Frohman-Bentchkowski, **Eli Harari**, George Perlegos, Fujio Masuoka, and the Intel team of **Stefan Lai**, Niles Kynett, Bruce McCormick and Richard Pashley



1967: Invention of the Floating Gate

- Dawon Kahng and Simon Sze at Bell Labs
- What would happen if a MOSFET was built with extra layers like the layers in a cake?



Phase Change Memory (PCM)

- 1969: Inventor: Charles Sie at Iowa State Univ.
 - 1 v. 0 stored via amorphous v. crystalline state
- 1970: early PCM work by Gordon Moore at Intel



Amorphous semiconductors Part I

Nonvolatile and reprogrammable, the read-mostly memory is here

Integrated arrays combine amorphous and crystalline technologies;
new memories could help realize promise of microprogramming

By R. G. Neale and D. L. Nelson, *Energy Conversion Devices Inc., Troy, Mich.*
Gordon E. Moore, *Intel Corp., Mountain View, Calif.*

- Late 80s: PCM used in Panasonic optical disks
- 1999: Stefan Lai started Intel alternative memory team
- **RUMOR**: Intel and Micron will use PCM in 3D XPoint technology



1970: Invention of the EPROM

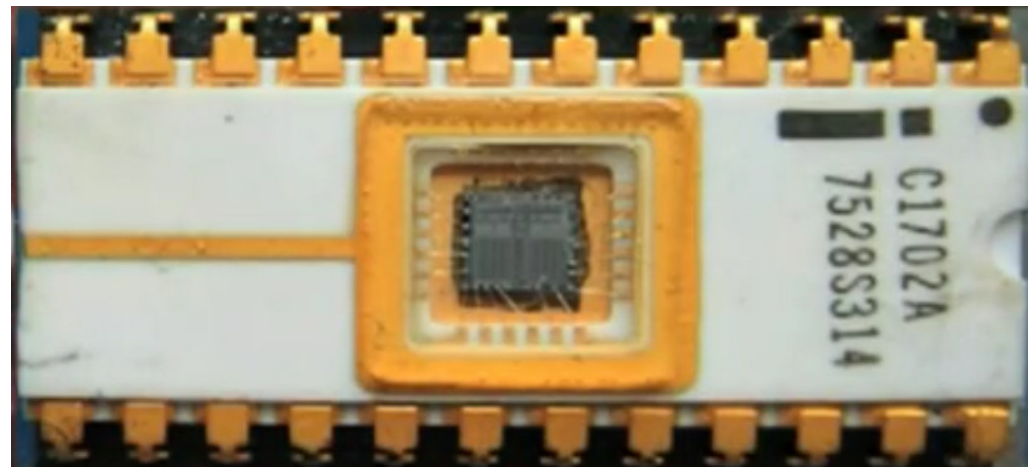
- Dov Frohman-Bentchkowski at Intel
- “FAMOS” transistor; erase entire device with UV light
- Rcvd. IEEE Edison Medal; Nat’l. Inv. Hall of Fame

MEMORY BEHAVIOR IN A FLOATING-GATE AVALANCHE-INJECTION MOS (FAMOS) STRUCTURE

D. Frohman-Bentchkowsky

Intel Corporation, 365 Middlefield Road, Mountain View, California 94040

(Received 28 December 1970)



1976: Harari – First EEPROM Patent

- 3/26/76: a functional EEPROM with **thin** SiO₂

United States Patent [19]

[11] **4,115,914**

Harari

[45] **Sep. 26, 1978**

[54] **ELECTRICALLY ERASABLE
NON-VOLATILE SEMICONDUCTOR
MEMORY**

[75] Inventor: **Eliyahou Harari**, Irvine, Calif.

[73] Assignee: **Hughes Aircraft Company**, Culver
City, Calif.

[21] Appl. No.: **770,346**

[22] Filed: **Feb. 22, 1977**

Related U.S. Application Data

[62] Division of Ser. No. 671,183, **Mar. 26, 1976.**

[51] Int. Cl.² **H01L 29/78**

conductor Memories" Session 4, 1972 Wescon Technical Papers.

Rapp; "Silicon on Sapphire" Electronics Products Magazine (1/15/73), pp. 83-84.

Primary Examiner—Gerald A. Dost

Attorney, Agent, or Firm—George Tacticos; W. H. MacAllister

[57] **ABSTRACT**

A non-volatile semiconductor storage device comprising a dual gate field effect transistor in which an electrically floating gate acts as a charge storage medium. An insulating layer of an appropriate dielectric material separates the floating gate from the active portion of the transistor. **A predetermined section of this insulating layer is relatively thin** to permit this section of the float-

ing only a dry oxygen ambient. **The resulting silicon dioxide layer 54 in opening 52 will have a thickness typically in the range of 20 to 100 Å.** The actual temper-

1976: Toshiba: EEPROM Paper (device never operational)

- Co-authored by Masuoka ('84: Flash inventor)
- “SAMOS” transistor with **2000 Å thick** SiO₂

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. ED-23, NO. 4, APRIL 1976

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Electrically Alterable Avalanche-Injection-Type MOS READ-ONLY Memory with Stacked-Gate Structure

HISAKAZU IIZUKA, FUJIO MASUOKA, TAI SATO, AND MISTUAKI ISHIKAWA

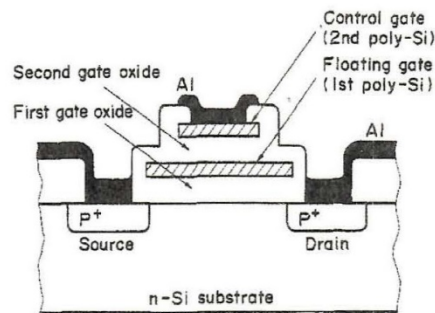


Fig. 1. Structure of a stacked-gate avalanche-injection-type MOS (SAMOS) memory transistor.

The drain avalanche-breakdown voltage under zero gate bias is -38 to -40 V for a gate oxide **2000 Å thick** before walk-out [8]. The electric field E_1 decreases linearly as increasing V_D [3].

side). Both of the gate-oxide thickness are **2000 Å**. Elemental parameters are as follows:

1976-77: Invention of a Practical and Reliable EEPROM

- Eli Harari at Hughes Microelectronics
- Experiments determined that thin SiO₂ (**90-100 Å**) was optimal for a practical, reliable and manufacturable EEPROM with proper endurance based on F-N tunneling



Dielectric breakdown in electrically stressed thin films of thermal SiO₂

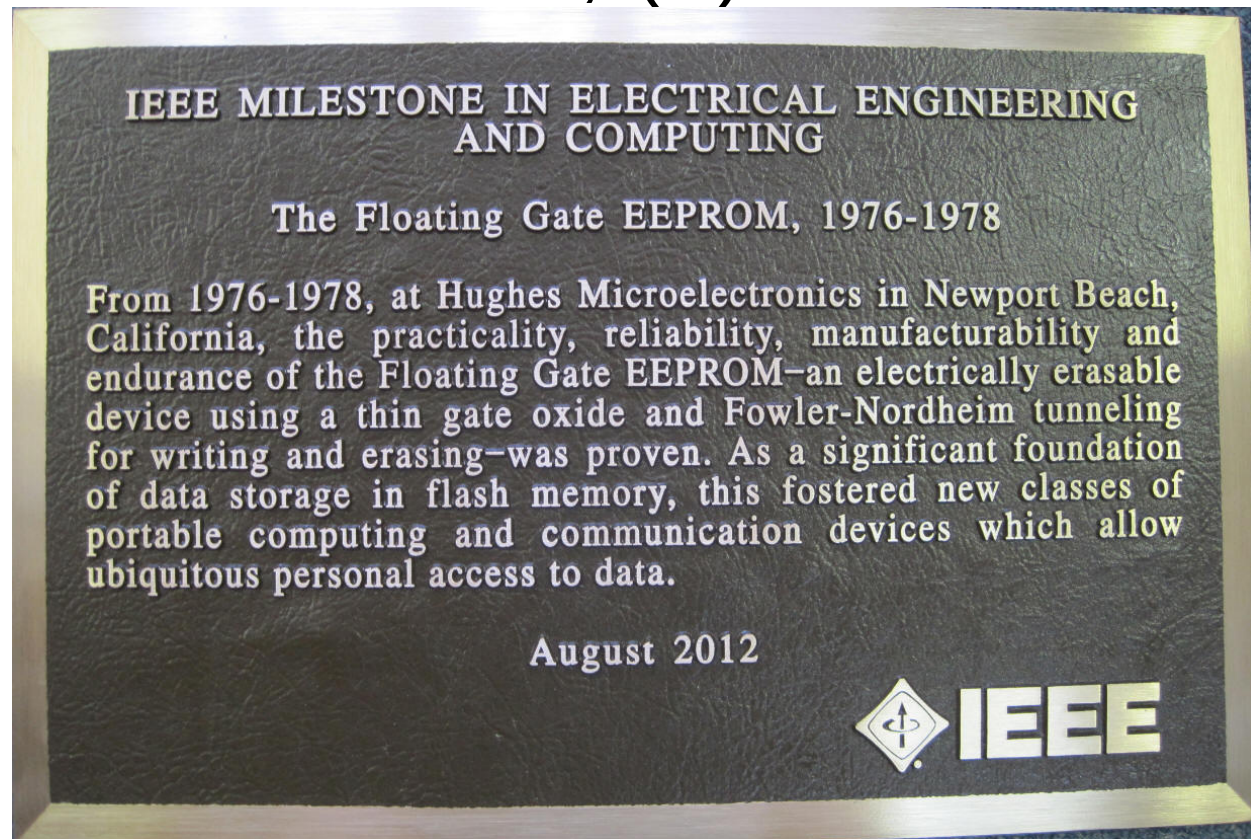
Eli Harari

Newport Beach Research Center, Hughes Aircraft Company, Newport Beach, California 92663
(Received 8 August 1977; accepted for publication 8 November 1977)

A novel technique is described which was used to study the intrinsic breakdown mechanism in films of thermal SiO₂ in the thickness range 30–300 Å. It was determined that high-field and high electron

Harari's FG EEPROM Recognized with IEEE Milestone in 2012

- Milestone recognizes how thin SiO₂ enabled (1) first practical FG EEPROM, (2) flash memory, and ultimately (3) data storage in flash memory



Intel / Xicor / SeeQ / Atmel (1 of 3)

■ George Perlegos

- 1974: joined Intel to work with Dov Frohman
- 1974: 1st NMOS EPROM (for 8080)
- 1975: 1st 5V-only EPROM (for 8085)
- 1977-78: created FLOTOX, the first commercially successful EEPROM



■ Intel still wanted to pursue EPROM, not EEPROM

- 1978: group led by Rafi Klein formed **Xicor** (“eX Intel Corp. company”) to pursue EEPROM
- Group included Julius Blank of Fairchild’s “Traitorous Eight”

Intel / Xicor / SeeQ / Atmel (2 of 3)

- Intel **still** wanted to pursue EPROM, not EEPROM
 - 1981: When team moved to Folsom, George Perlegos, Phil Salsbury, Gordon Campbell quit
- They formed **SeeQ**
 - “EE is our middle name”
 - Solved EEPROM’s high voltage requirement
 - Plus: new EEPROM as easy to use as SRAM
 - Minus: expensive, slow, limited endurance
- SeeQ thrived, expanded into logic products

Intel / Xicor / SeeQ / Atmel (3 of 3)

- 1984: George Perlegos left SeeQ
 - Formed Chips and Technologies
 - Left C&T and formed **Atmel**
- Atmel
 - Developed:
 - CMOS EEPROM (first such device from Hughes in '81)
 - Intel-compatible CMOS EPROM
 - Late '80s: NOR Flash
 - Early '90s: 1st Flash Microcontrollers (very successful)
 - 1994: acquired SeeQ's EEPROM business
 - Likely to be acquired by UK-based Dialog Semi

Fujio Masuoka

- 1971: 1st job at Toshiba
- Tasked with EPROM development in wake of Dov Frohman's single-gate EPROM ISSCC paper
- 1973: gave ISSCC paper on double-gate EPROM w/ 100x faster programming time
- Mid '70s to early '80s: DRAM investigation



Masuoka: NOR Flash

- 1984: IEDM paper introduced NOR Flash
 - First simultaneously erasable NV memory
 - An entire chip could be erased at once, like the “flash” of a camera

Characteristic	EEPROM	Flash EEPROM
Transistors/cell	2	1
Programmability	Byte	Byte
Erasability	Byte	Entire Device
2 Micron Lithography	272 sq. microns	64 sq. microns
	F-N tunneling	Hot electron injection (as proposed)

Fujio Masuoka: NAND Flash

■ 1986

- TI filed patent infringement suit against Toshiba re: DRAM products
- Masuoka testified at International Trade Commission (ITC) trial in Wash., DC
- Was bored during trial
- He spent idle time thinking about NAND Flash
- Wrote 5 NAND Flash patents during this time



■ 1987: NAND Flash published in IEDM Paper

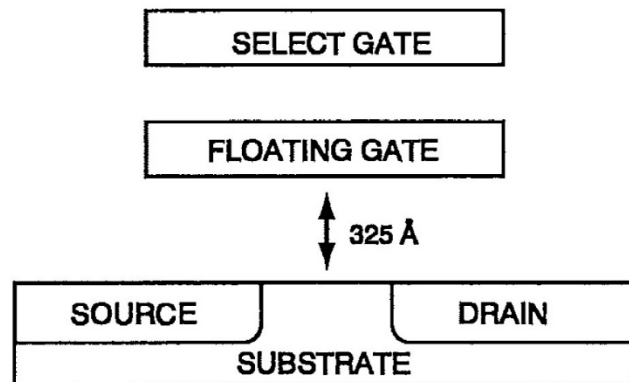
Stefan Lai's Journey

- Joined Intel in 1982
- EPROM was a big business for Intel
- Most key EPROM people had left for startups
 - 1978: Rafi Klein and crew left + formed Xicor
 - 1981: when EPROM team moved to Folsom, George Perlegos and crew left + formed SeeQ
 - 1981: Eli Harari left, telling Gordon Moore:

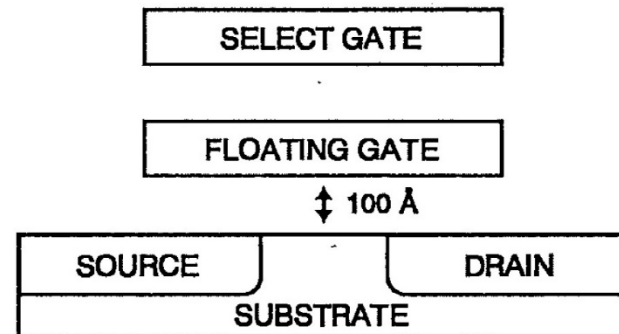
“Some form of EEPROM will replace EPROM, so pursue EEPROM aggressively!”

Stefan Lai: NVM Work at Intel

- When hired: find out how to scale EEPROM
 - Wanted a simple and practical EEPROM
- Looked to ETOX (EPROM Tunnel Oxide)
 - Conceived at Intel in late 1983 (another EEPROM project had failed)
 - ETOX used thin SiO₂ (100 Å):



EPROM CELL



ETOX FLASH CELL

Stefan Lai: NVM Work at Intel

- Mid-1984:
 - ETOX working cell demonstrated
 - E2EPROM (electrically erased EPROM with byte erasure) was proposed, but the Intel business unit wanted EEPROM
- 8/85: Intel teams with Xicor for EEPROM using triple polysilicon tunneling
- ETOX continued as a “skunk” works project
 - Supported by Dick Pashley, GM of new E2 business unit

ETOX: NOR Flash Instead of EEPROM

- 1987 (after 2 years):
 - Xicor and ETOX projects both successful
 - Xicor required 3 transistors/cell
 - ETOX economics best; Xicor program killed
- ETOX Productized as 256Kb NOR Flash
 - Late '87: samples / Early '88: ISSCC paper
 - 4/88: formal product intro in Paris
 - Demo: digital photos stored in proprietary flash cards
 - Block-erasable device at 1.5 μm

ETOX's Success

- 1987-91:
 - ETOX NOR Flash quadruples every year
 - 1991 sales: about \$100M
- 9/89:
 - Psion introduces the world's first Flash Card-based Mobile Computer
 - Joint Intel (Flash Memory) / Microsoft (Flash File System Software) announcement
- 2/92:
 - Intel and Sharp are mfg. and development partners for 2 product generations

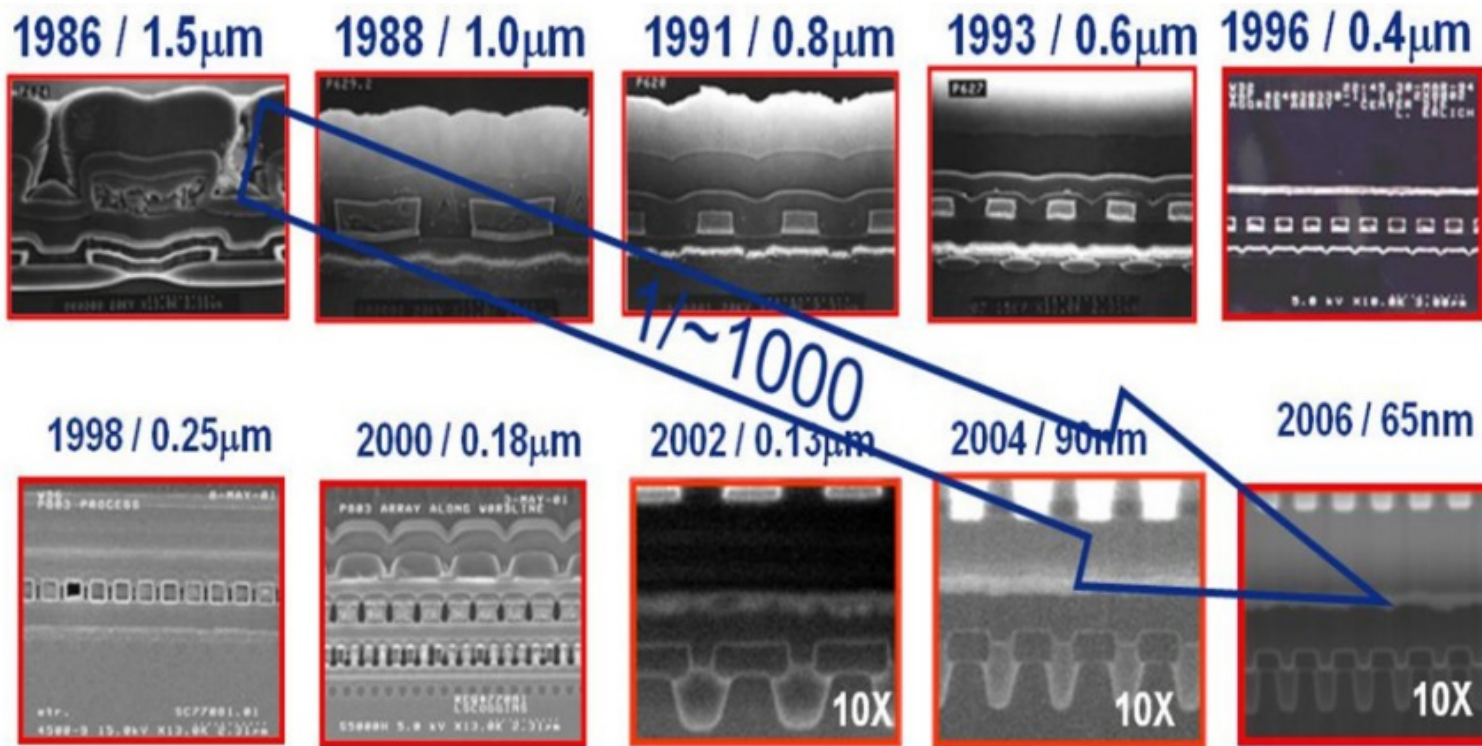
ETOX MLC Product

■ 2/95: ISSCC

- First paper re: a Multi-Level Cell (MLC) product
 - MLC is >1 bit per FG transistor
- M. Bauer, R. Alexis, G. Atwood, B. Baltar, A. Fazio, K. Frary, M. Hensel, et al.: *A Multilevel-Cell 32Mb Flash Memory*

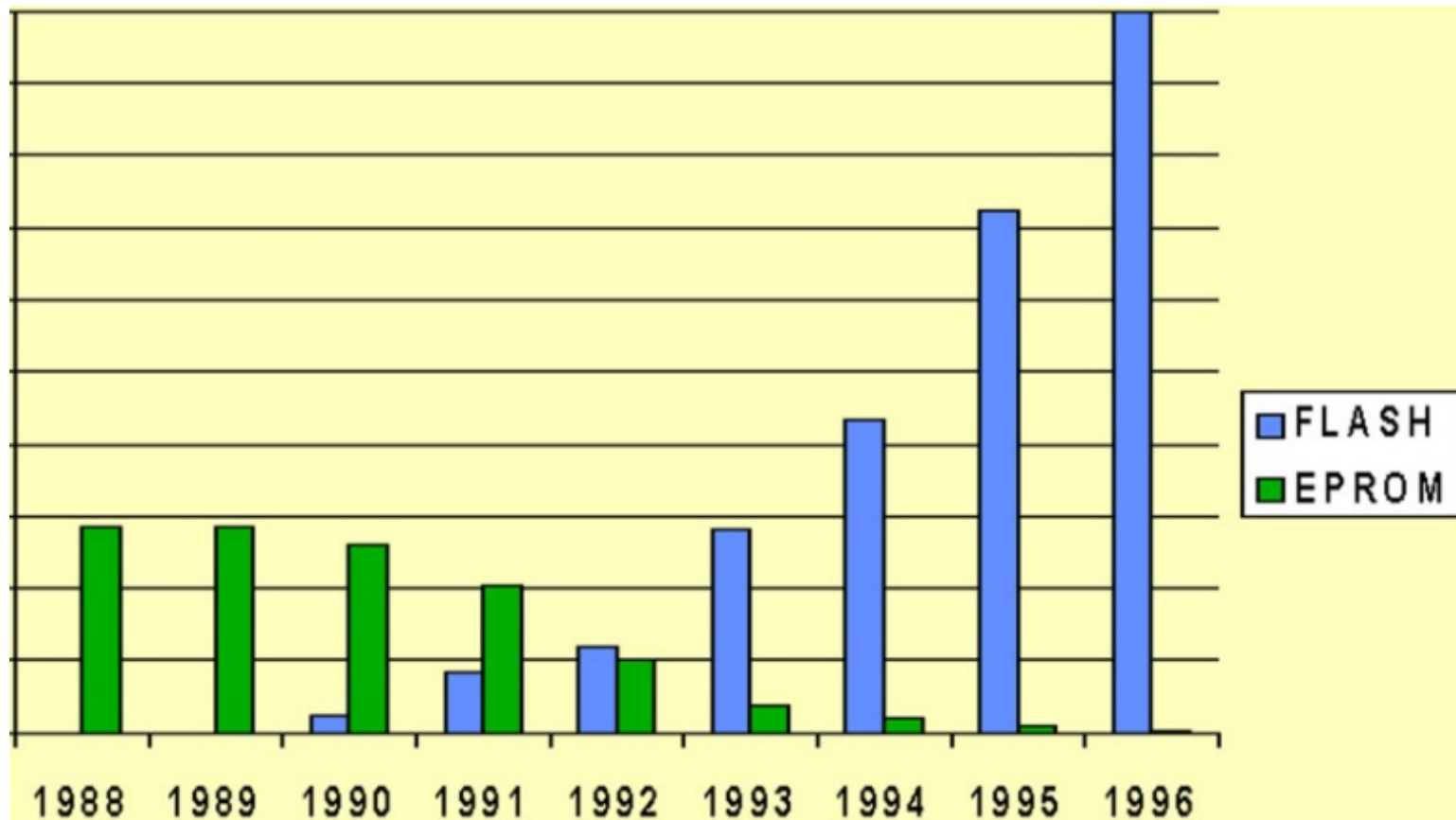
1986-2006: ETOX NOR Cell Shrinkage Over 10 Generations (800x)

- 1986: 36 sq. μm ; 2006: .0457 sq. μm



Volume Production Year / Technology Generation, Source: Intel

Intel: EPROM v. NOR Flash Sales



Eli Harari's Goal: Solid State Disk (SSD) - Mass Storage in Silicon

- 1979: Dov Frohman hires Eli at Intel
- 1981: EEPROM SSD proposal while at Intel
 - Rejected by CEO Andy Grove
- 1983-88: Wafer Scale Integration
 - Co-founder; Goal: WaferDisc: EEPROM SSD
- 3/1/88: Founded SunDisk (renamed SanDisk)



S O L I D - S T A T E M A S S S T O R A G E S Y S T E M S

SunDisk

Eli Harari's Goal: Solid State Disk (SSD) - Mass Storage in Silicon

- 6/8/1988: filed patent application
 - MLC: > 1 bit per FG (Intel MLC NOR in '95)
 - Intelligent erasure for high endurance
 - Flash SSD to emulate magnetic HDD

Patent Number: 5,095,344

Date of Patent: Mar. 10, 1992

HIGHLY COMPACT EPROM AND FLASH EEPROM DEVICES

Inventor: Eliyahou Harari, 2320 Friars La.,
Los Altos, Calif. 94022

Appl. No.: 204,175

Filed: Jun. 8, 1988

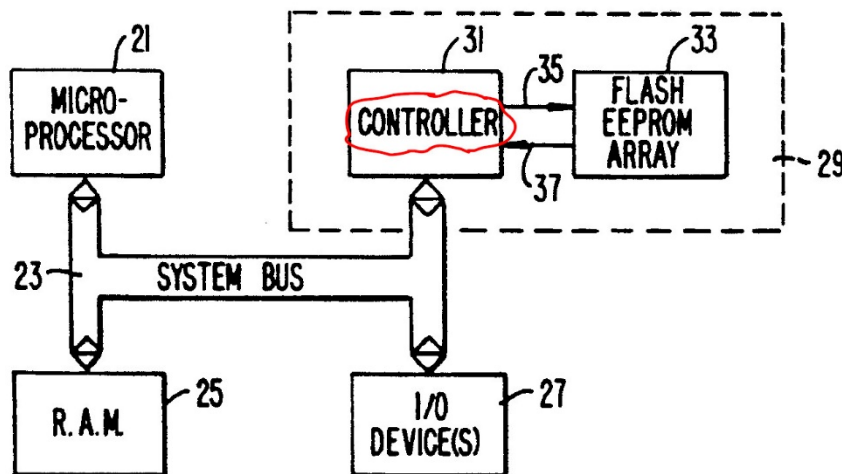
[57]

ABSTRACT

Structures, methods of manufacturing and methods of use of electrically programmable read only memories (EPROM) and flash electrically erasable and programmable read only memories (EEPROM) include split channel and other cell configurations. An arrangement of elements and cooperative processes of manufacture provide self-alignment of the elements. An intelligent programming technique allows each memory cell to store more than the usual one bit of information. An intelligent erase algorithm prolongs the useful life of the memory cells. Use of these various features provides a memory having a very high storage density and a long life, making it particularly useful as a solid state memory in place of magnetic disk storage devices in computer systems.

System-Flash

- 4/13/1989: filed patent application
 - “System-Flash”
 - Intelligent flash management with CPU and firmware



FLASH EEPROM SYSTEM

Inventors: **Eliyahou Harari**, Los Gatos; **Robert D. Norman**, San Jose; **Sanjay Mehrotra**, Milpitas, all of Calif.

Assignee: **SunDisk Corporation**, Santa Clara, Calif.

Appl. No.: **963,838**

Filed: **Oct. 20, 1992**

Related U.S. Application Data

Division of Ser. No. 337,566, **Apr. 13, 1989**, aban-

[57]

ABSTRACT

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

System-Flash

- Architecture included:
 - Error correction and dynamic defect mapping
 - Wear-leveling
 - Logical-to-physical mapping
 - Low stress write and erase voltages
 - Intelligent caching: speed, and write reduction
 - Garbage collection
 - Repair of disturbed cells
 - Magnetic disk drive interface
- **Key feature: Data Header**
 - “Overhead data” to allow management

Getting System-Flash to Market

- Marketplace acceptance criteria:
 - Host-independent plug-compatible disk drive replacement
 - 1 million read/write cycles
- Criteria only possible with:
 - Dedicated hardware controller and firmware
 - High-endurance flash with embedded header
 - Stress of write/erase voltages controlled by header data
- Mass acceptance required price reduction
 - MLC Flash (multi-bits/cell)
 - Switch from NOR to higher-density NAND
 - Moore's Law

First ATA SSD

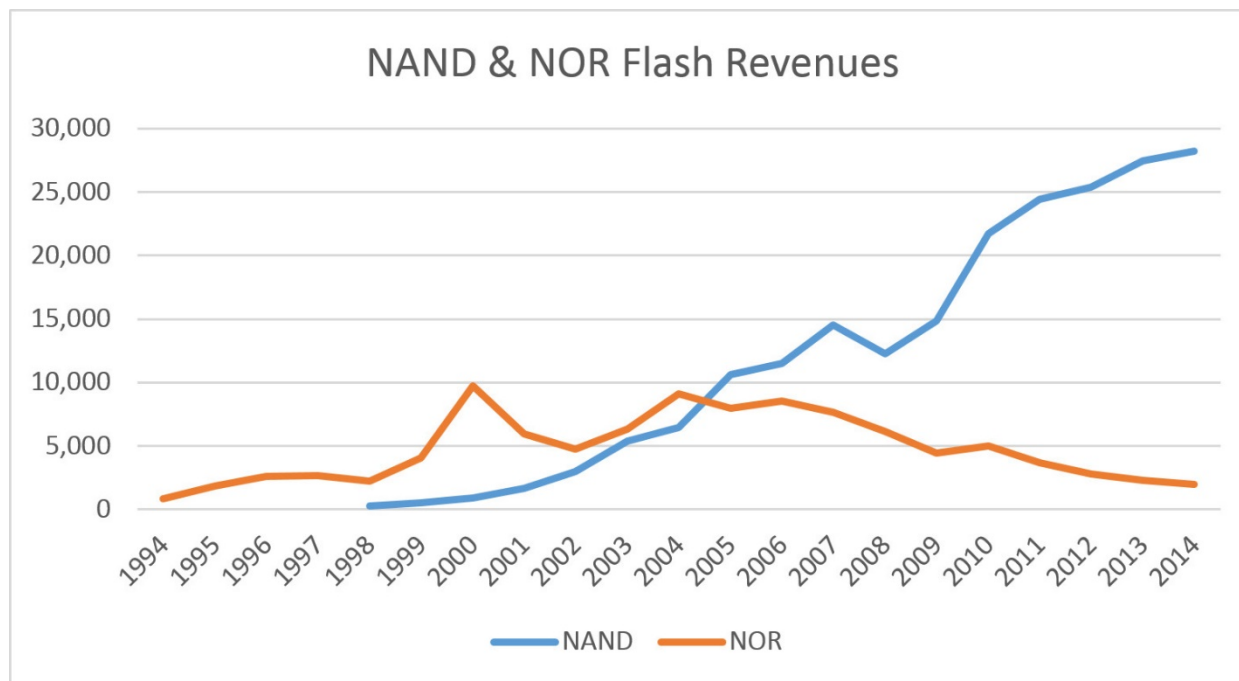
■ 1991: First ATA SSD

- 20MB; \$1000
- ATA device
- 2.5" form factor
- 1st customer:
 - GRiD for GRiDPad pen computer
- IBM:
 - Contract for HDD replacement for 10,000 ThinkPads



Flash Sales: NOR v. NAND

Sales in \$B	1994	1998	2000	2003	2014
NOR	.865	2.20	9.71	6.35	2.00
NAND		.285	.924	5.39	28.23
Total	.865	2.49	10.64	11.74	30.24



Cellphones: The Impact of Flash

- Early '90s: first use of NOR flash for updatable firmware
- 1997/98: first use of NAND in MMC flash memory cards
- 2001: first internal NAND: Nokia 9100 smartphone
- 2007: iPhone introduction
- Today: cell phones use nearly 30% of NAND flash production



SANDISK MULTIMEDIACARD FOR MOBILE PHONES

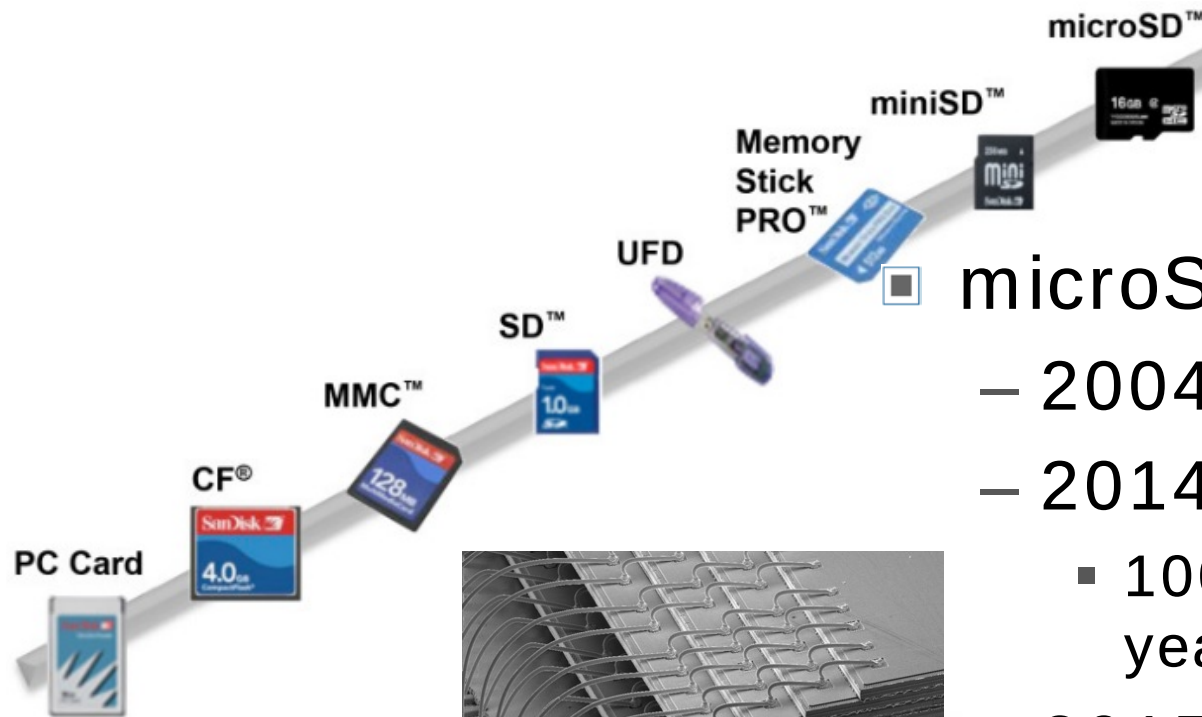
SanDisk's new MultiMediaCard (MMC), the world's smallest solid state storage device, is expected to emerge as a new portable storage standard for mobile phones, pagers and other small handheld systems. Leading telecommunications companies support MMC. (SanDisk photo)



Nokia 6600

Portable Data Storage: Cards + Sticks

- 1991: PCMCIA flash cards



- microSD card

- 2004 (128MB)
- 2014 (128GB)
 - 1000x increase in 10 years
- 2015 (200GB)
 - 16 stacked flash chips
 - TLC (3 bits/cell)

Apple iPod: From HDD to Flash

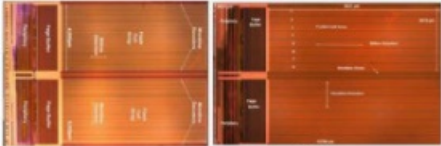
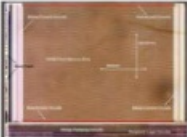
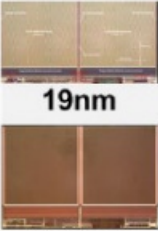
- 2000: Steve Jobs met with Eli Harari
 - Wanted SSD at Toshiba HDD price
- Oct. **2001**: iPod introduced
 - 5GB Toshiba 1.8" HDD
- Jan. 2004 - Sept. 2005: iPod Mini
 - 4GB/6GB 1" Microdrive from Hitachi and Seagate (used CompactFlash i/f)
- Sept. **2005**: iPod Nano
 - 4GB flash
- Current models: 16GB flash



Four NAND Flash Manufacturers

TECHINSIGHTS

NAND Flash Products

Makers	20 nm Class (2D)	10 nm Class (2D)	3D NAND
	 27nm 21nm	 19nm	 V-NAND (24 L → 32L)
	 24nm	 19nm A-19nm	 15nm
	 25nm 20nm	 16nm	
	 26nm	 16nm	

Samsung's 3rd Generation 3D NAND

Samsung 3D V-NAND

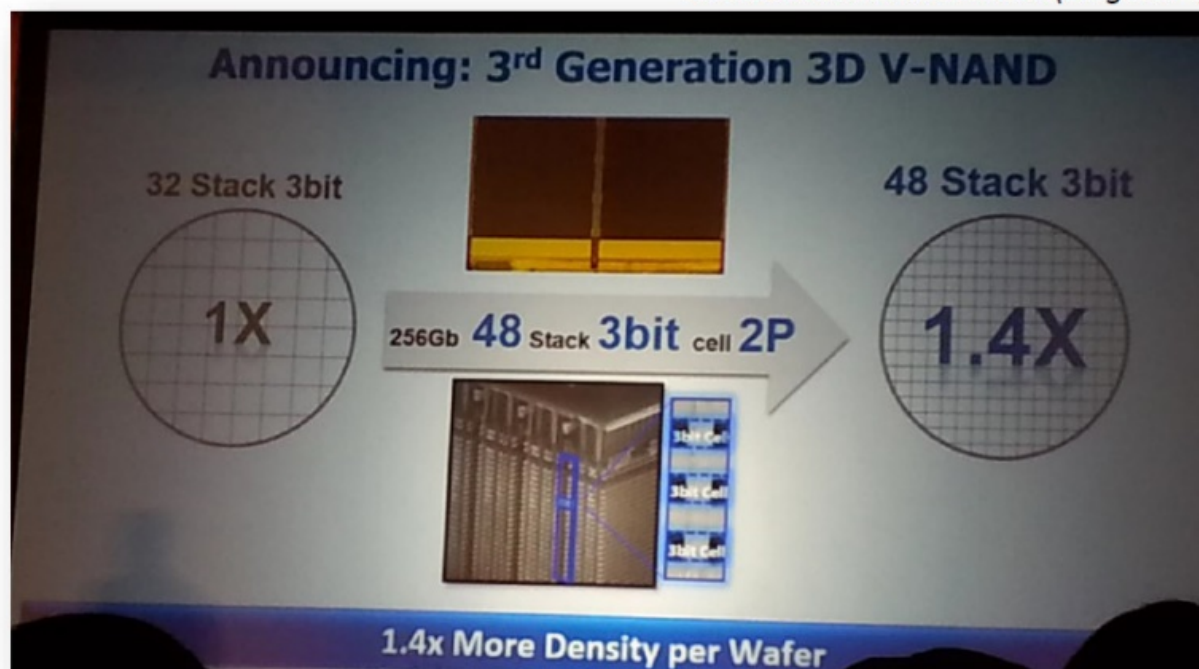
TECHINSIGHTS

1st Generation (V1, 2012 ~ 2013): 24 Layers/128Gb

2nd Generation (V2, 2014 ~ 2015): 32 Layers/128Gb

3rd Generation (V3, 2015 3Q ~ 2016): 48 Layers/256Gb

Announced at FMS2015 (Aug. 11th)

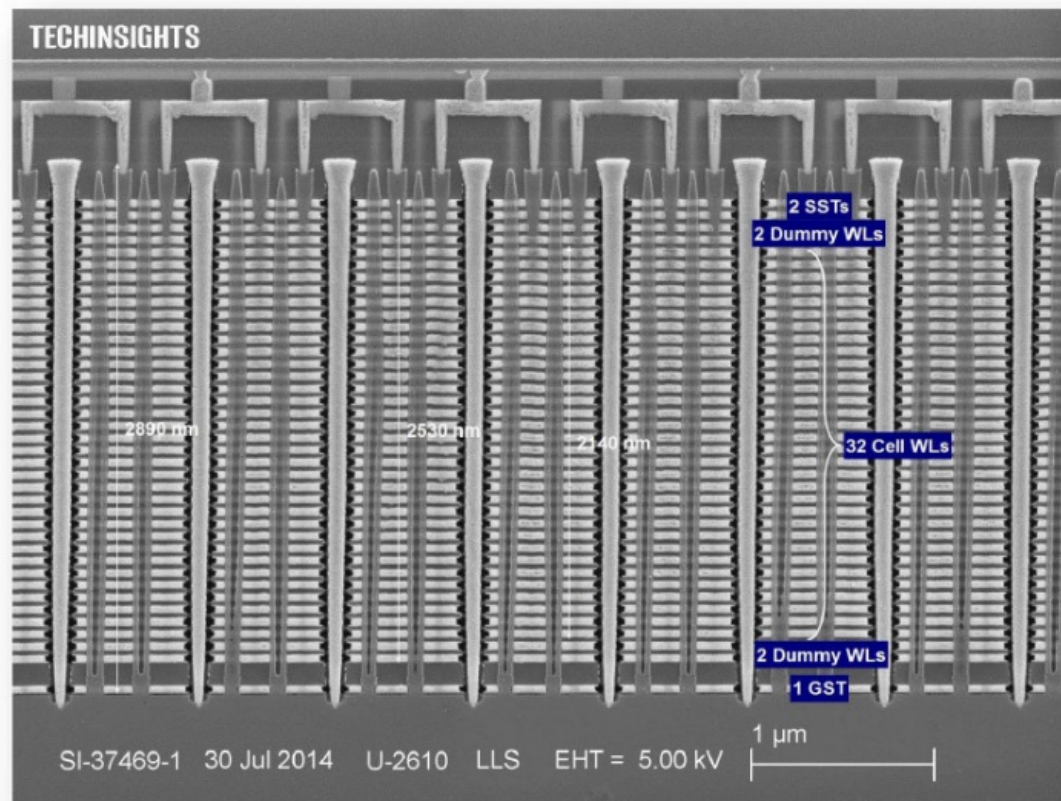


Samsung's 2nd Gen. 3D NAND

Samsung 3D V2-NAND

TECHINSIGHTS

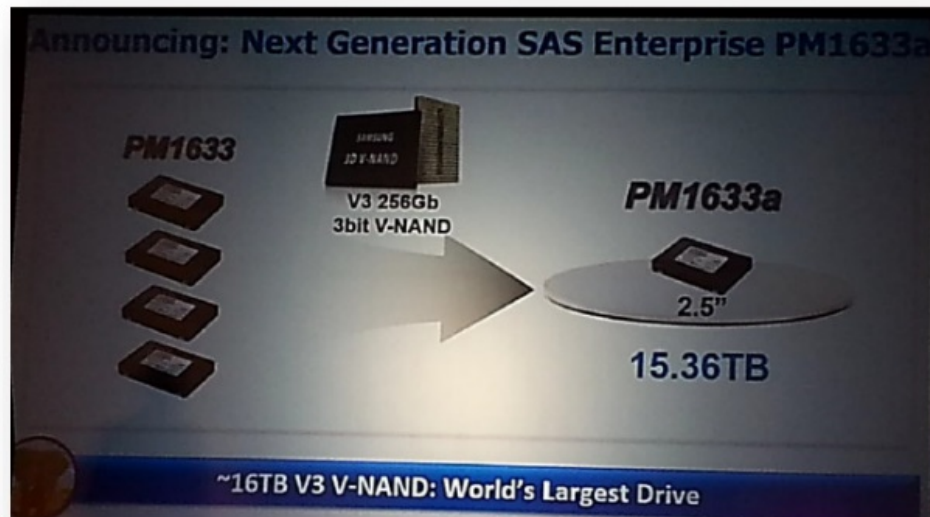
V2-NAND 32 Layers (X-section)



3D NAND Products

Samsung PM1633a (3D V3-NAND)

TECHINSIGHTS



PM1633a (15.36 TB) to ship early 2016



PM1725, a one million IOPS 6.4TB NVMe PCIe SSD